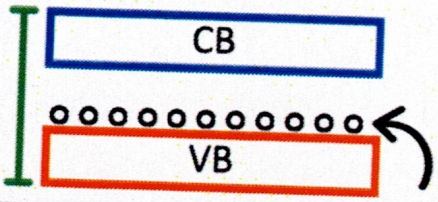
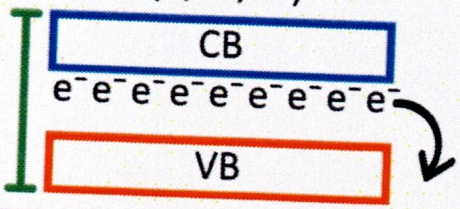
SEMICONDUCTORS

Classification of Semi-conductors

Extrinsic Semiconductors

P-type	N-type
Trivalent impurity is added (B,In,Al) 	Pentavalent impurity is added (P,As,Sb) 
$n_h >> n_e$	$n_h << n_e$
$J \cong en_hV_h$	$J \cong en_eV_e$
$\sigma = \frac{1}{\rho} \cong en_h\mu_h$	$\sigma = \frac{1}{\rho} \cong en_e\mu_e$

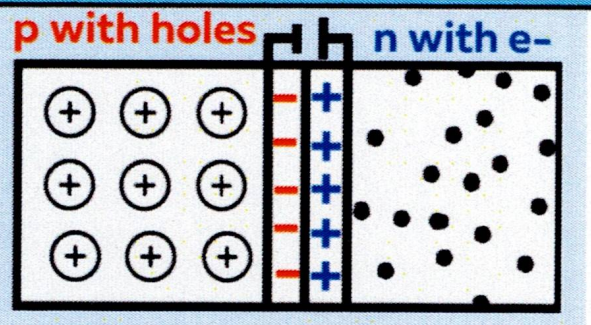
Intrinsic Semi-conductors

$Si \rightarrow E_g = 1.1\ eV$ $Ge \rightarrow E_g = 0.68\ eV$ $n_e = n_h = n_i$	Conductivity of Semiconductors $\sigma = e(n_e\mu_e + n_h e\mu_h)$
$J = ne[V_e + V_h]$	$\sigma = \frac{1}{\rho} = en[\mu_e + \mu_h]$

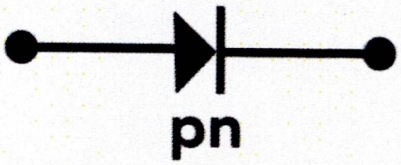
Mass Action Law

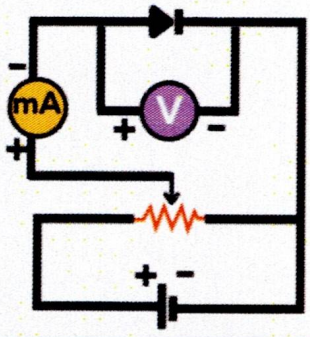
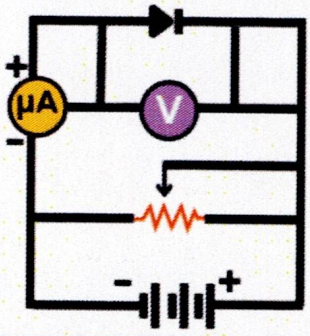
$n_1^2 = n_hn_e$	$n_1^2 \rightarrow$ intrinsic carrier density

P-N Junction diode or Semi Conductor diode

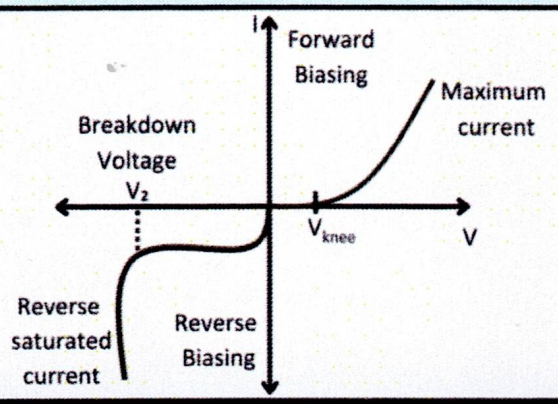


P-N junction diode



Forward Biasing	Reverse Biasing
	
p end →connected with higher potential	p end →connected with lower potential
n end →connected with lower potential	n end →connected with higher potential
depletion layer decreases	depletion layer increases
$V_p > V_n$ $V_p - V_n$ = positive	$V_p < V_n$ $V_p - V_n$ = negative
Forward current flows in circuit	Reverse current flows in circuit

Characteristic Graph



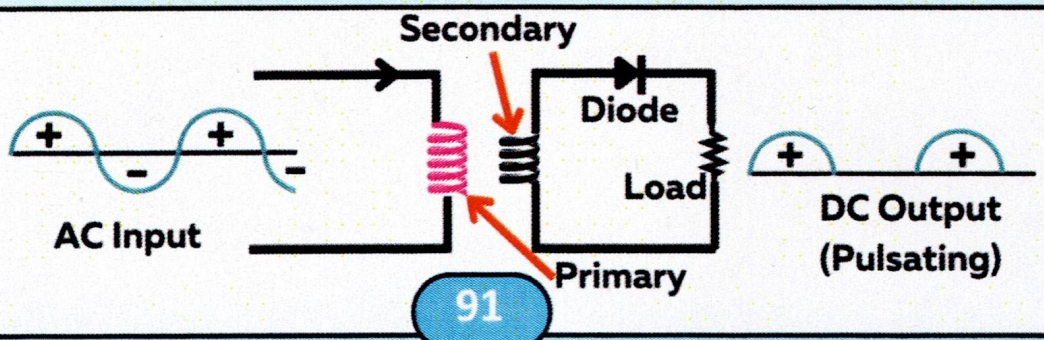
Behaviour in Circuit

Ideal Diode		Real Diode	
Forward Bias	Reverse Bias	$S_i \rightarrow V_{knee} = 0.7$ $G_e \rightarrow V_{knee} = 0.3$	
$R \rightarrow 0$	$R \rightarrow \infty$	Forward Bias	Reverse Bias
Short circuit	Open circuit	Current flow from p to n	Current flow from n to p
$V_{knee}=0$	$V_{knee}=0$		
$I = \frac{V_{ext}}{R_{ext}}$	No current will flow	$I = \frac{V_{ext} - V_{knee}}{R_{ext} - R_f}$	No current passed

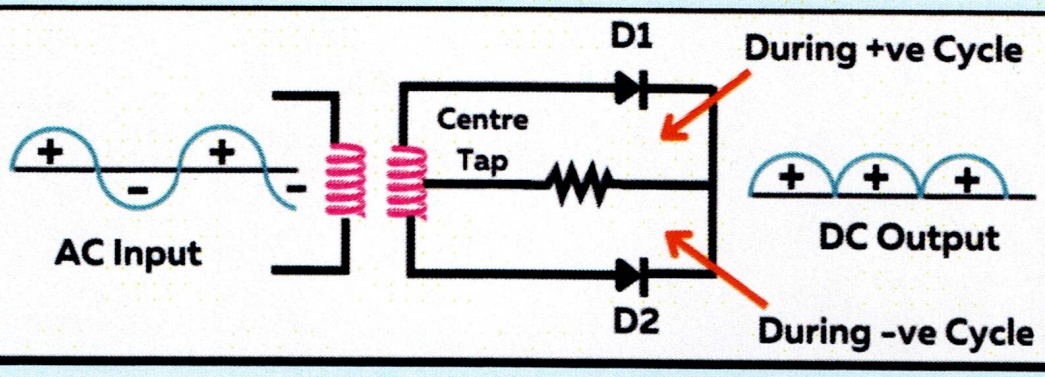
Application of p-n junction diode

Rectifier	Converts AC input to DC output

Half-Wave Rectifier



Full-Wave Rectifier

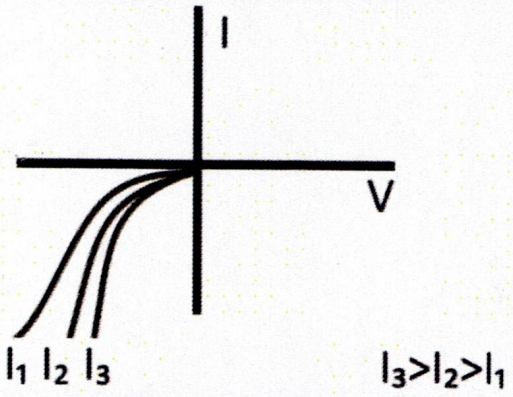


Light Emitting Diode

Less Power Consumption/Power losses/Heat losses	$\lambda_{emit} = \frac{12400}{E_g} A^{\circ} \cong 100A^{\circ} - 500A^{\circ}$

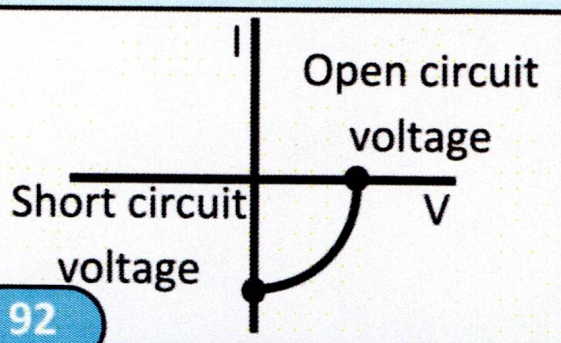
Photo Diode

- Normal diode in reverse biased
- Used for detection of light



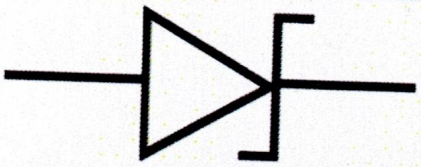
Solar cell

No Biasing



Zener Diode

It is used as voltage regular when used as reverse biased



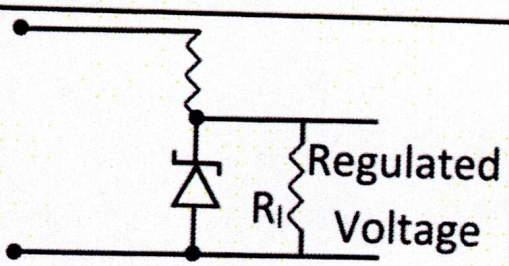
Case (i) = $V_{ext} < V_z$

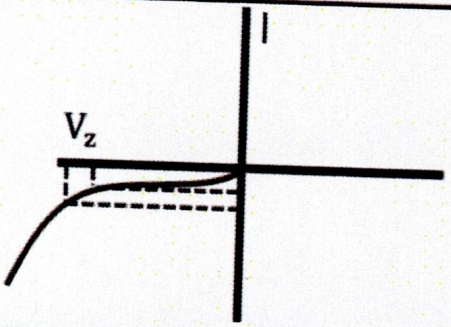
Behave as real diode

Case (ii) = $V_{ext} \geq V_z$

V_z will be fixed voltage

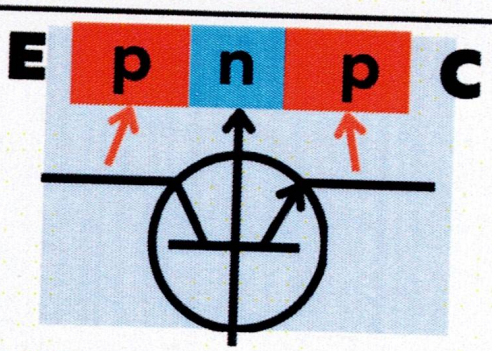
$P_z = V_z I_z$

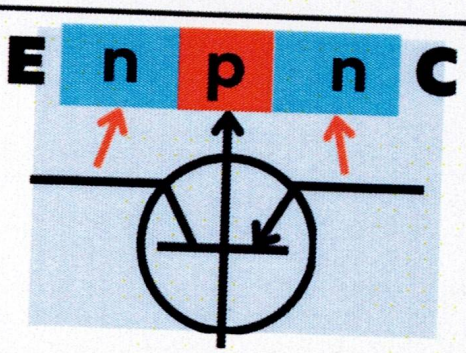




Transistors

Two junctions, Three terminal diodes

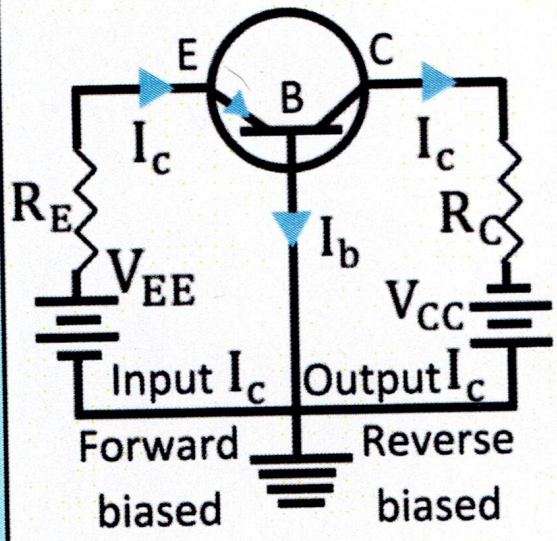
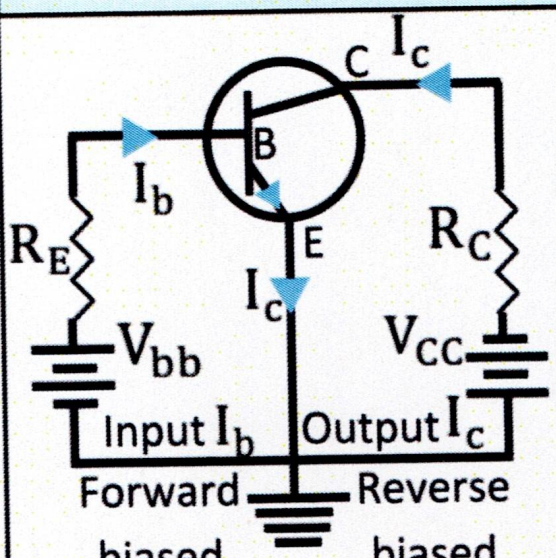




$I_E = I_b + I_c$

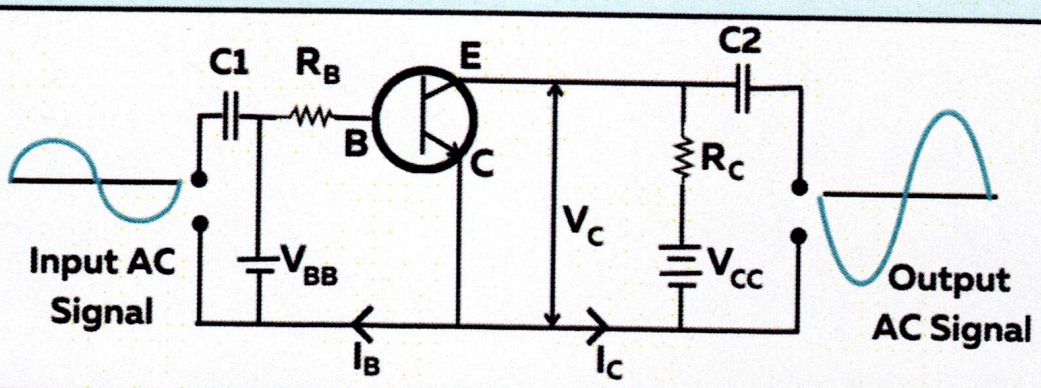
$I_b \cong 5\% I_E$

$I_c \cong 95\% I_E$

Common Base		Common Emitter	
			
Current Gain	$\alpha = \frac{I_C}{I_E}$	**Current Gain**	$\beta = \frac{I_C}{I_b}$
Voltage Gain	$\alpha \frac{R_C}{R_E}$	**Voltage Gain**	$\beta \frac{R_C}{R_b}$
Power Gain	$\alpha^2 \frac{R_C}{R_E}$	**Power Gain**	$\beta^2 \frac{R_C}{R_b}$
Phase	Same phase	**Phase**	Opp. phase
Relation b/w α & β			
$\alpha = \frac{\beta}{\beta + 1}$		$\beta = \frac{\alpha}{1 - \alpha}$	

Transistor as a device

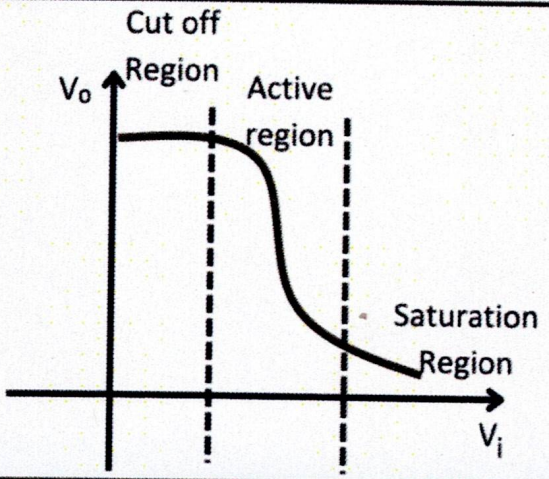
As an amplifier



With increase in input voltage (beyond 0.6V) I_c increases and V_0 decreases (Active State)

As a Switch

With increase in input voltage (0-0.6V) $V_0 = V_{CC}$ max (off state) Non Conducting transistor	I_c becomes max, output voltage decreases slowly (ON) Stage



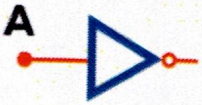
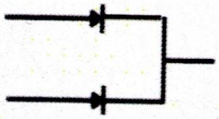
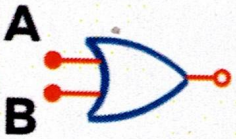
Logic Gates

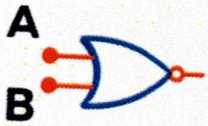
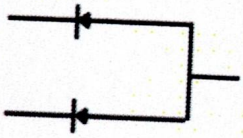
De Morgan Law

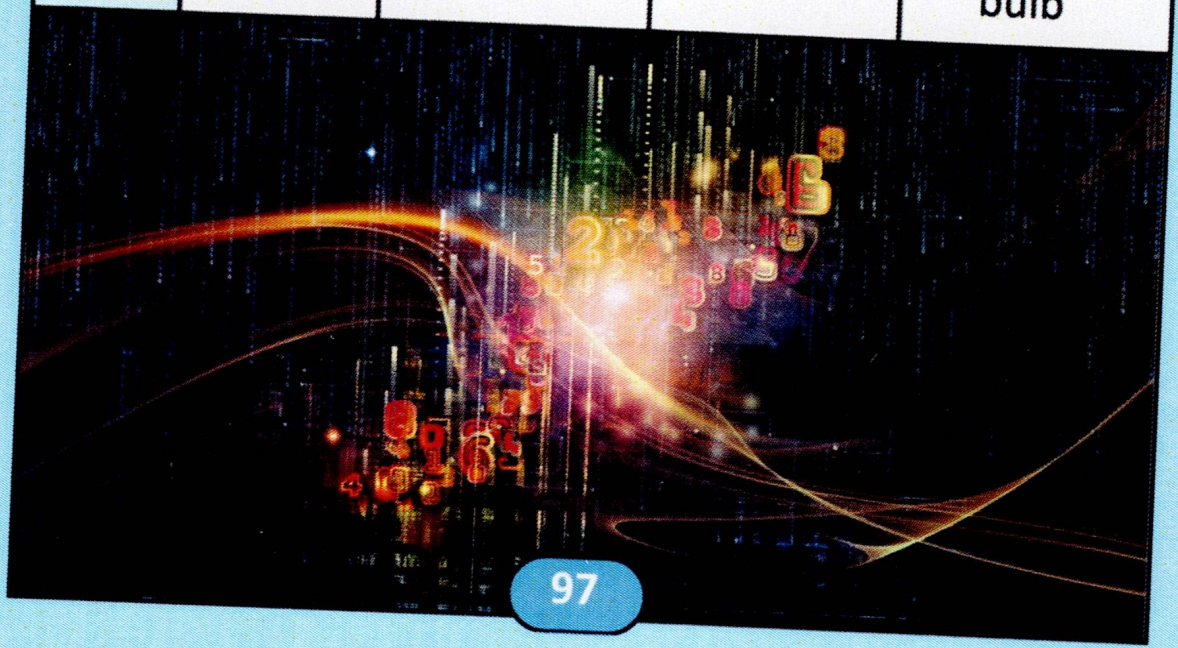
$\overline{A+B} = \overline{A}.\overline{B}$	$\overline{\overline{A}+\overline{B}} = AB$
$\overline{AB} = \overline{A}+\overline{B}$	$\overline{\overline{AB}} = A+B$

Different Combinations

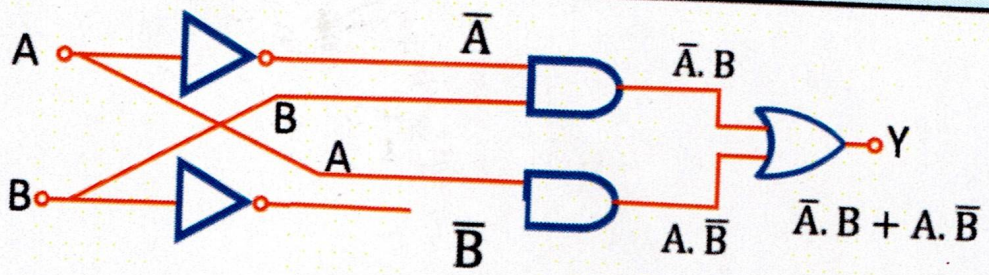
Input		OR	NOR	AND	NAND	X-OR	X-NOR
A	B						
0	0	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	1	0	1	0	0	1

Gate	Boolean Expression	Formed Using	Circuit Symbol	Electrical Circuit
NOT	$Y = \overline{A}$	CE Transistor		Key parallel with bulb
OR	$Y = A + B$			Two keys in parallel and in series with bulb

Gate	Boolean Expression	Formed Using	Circuit Symbol	Electrical Circuit
NOR	$Y = \overline{A + B}$	Diode + CE Transistor		Two keys in parallel and in parallel with bulb
AND	$Y = A.B$			Two keys in series and in series with bulb
NAND	$Y = \overline{A.B}$	CE + two diode		two keys in series and in parallel with bulb



Exclusive-OR/XOR

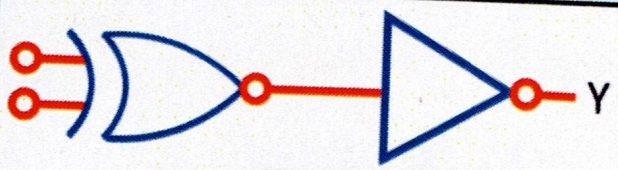


$$Y = \bar{A}.B + A.\bar{B}$$

Symbol	

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive- NOR



$$Y = \overline{\bar{A}.B + A.\bar{B}}$$

A	0	0	0	1
B	0	1	0	1
Y	1	0	0	1